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EXAMINER	
MONDT, JOHANNES P	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,484	DENG ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *36-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Response filed 3/12/04 to Election/Restriction Requirement mailed 12/16/03 indicates Applicant elects Species 3 and contains the statement that "claims 1, 21, 26 and 36 are generic". Applicant traverses on the grounds that "Species 1 is a transistor test structure", "Species 2 is a transistor design structure". However, the Species 1-3 clearly distinguish in the steps of the method in aspects tied to device definition differences. While the examiner agrees with the generic character of Species 1 with regard to claims 1-35 none of claims 36-46 read on elected Species 3, as neither the processor nor the memory as claimed therein are covered by Species 3. Therefore, claims 1-35 are being examined and claims 36-45 are withdrawn from consideration. Therefore, the traverse is rejected and the Election Requirement is made FINAL.

Claim Objections

1. ***Claim 31*** is objected to because of the following informalities: the term "select" (line 11) should be replaced by: "desired". Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. ***Claim 15*** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, "spacing between the body and the source-drain active area" is indefinite because said "body" lacks antecedent basis while according to

the terminology in the art of semiconductor devices both source and drain abut the body, implying the absence of the claimed spacing.

2. ***Claim 16 and dependent claims 17-20*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, with regard to lines 2-3 "calibration structure" by virtue of being a structure may have boundaries but only a mathematical model thereof can comprise boundary conditions. Therefore, said calibration structure cannot be consistently a structure nor a model of a structure, which renders claim 16 and claims 17-20 dependent on claim 16 indefinite.

3. The term "elaborate" on line 2 in ***claim 20*** is a relative term, which renders the claim indefinite. The term "elaborate" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

4. ***Claim 25*** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, "spacing between the body and the source-drain active area" is indefinite because said "body" lacks antecedent basis while according to the terminology in the art of semiconductor devices both source and drain abut the body, implying the absence of the claimed spacing.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-2, 4-6, 8-10, 12, 26, 29, 31- 33 and 35*** are rejected under 35 U.S.C. 102(b) as being anticipated by Gaston et al (Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Volume 8, March 1995). Gaston et al teach a method of determining a capacitance for use in a circuit simulation, the method comprising: determining a test structure capacitance of a test structure (the true M_2/M_1 capacitance in a ULSI integrated circuit; see pages 157-158, particularly second column of page 157 and first paragraph as well as final paragraph of the first column of page 158); simulating a design structure (using simulation program RAPHAEL which is by definition and capabilities a simulation package for the simulation of (parasitic) capacitance in a design structure; see final paragraph of page 159); extracting a design structure capacitance of the design structure (because that is what a parasitic simulation program as applied here to capacitance (see final paragraph of page 159) does); and calculating the parasitic capacitance of the design structure (see fourth sentence of final paragraph of page 159). Because the parasitic capacitance aimed at here is the capacitance other than the true M_2/M_1 capacitance obtained through FIB measurements (final paragraph of first column of page 158) and the parasitic capacitance is that part of the capacitance that is the contribution from neighboring conductive portions of the device interacting

over distance the parasitic capacitance is obtained by deducting the test structure capacitance from the design structure capacitance. In conclusion, Gaston et al anticipate claim 1.

On claim 2: the method by Gaston et al comprises providing a test structure (ULSI integrated circuit; see column 1 of page 157, third paragraph); simulating the test structure (see the third and fourth sentence of second column of page 159); extracting a test structure capacitance of the simulated test structure (namely: the parasitic capacitance of said test structure (final paragraph of second column of page 159).

On claim 4: the method by Gaston et al, in particular the determination of the test structure capacitance, comprises physically testing the test structure (through FIB as applied to the dielectric layer; see page 158, first column, final paragraph).

On claims 5-6: the method by Gaston et al, in particular the determination of the test structure capacitance, comprises selecting, based on the design structure, a test structure capacitance from a plurality of empirical test structure capacitances (cf. Table 1 and "Determination of Optimum Structure", page 158), each of the empirical test structure capacitances being determined by physically testing one of a plurality of different test structures (the capacitors corresponding to the tabulated plurality of capacitances through FIB; see "Determination of Optimum Structure", loc.cit.). Since said empirical test structures are also design structures by virtue of being input in the design simulations (cf. "Determination of optimum structure", page 158, second column, last sentence but one) claim 6 is met as well.

On claim 8: because Gaston et al determine an empirical device capacitance by physically testing the test structure (through FIB measurement of the thickness of the dielectric in the M2/M1 capacitor structure for a given test structure; see page 158, first column, final paragraph), and because a capacitance design *simulation* (cf. page 159, second column, final paragraph) results inherently in the total capacitance of the design structure, the total capacitance being by definition of the parasitic capacitance equal to the sum of the empirical device capacitance and the (total) parasitic capacitance the further limitation of claim 8 is met.

On claim 9: the test structure by Gaston et al is a ULSI CMOS integrated circuit and therefore said test structure by Gaston et al inherently comprises a gate, a source-drain active area (namely: the channel), a contact (namely: a contact to source and a contact to drain), a gate contact capacitance between the gate and the contact, and a gate to metal capacitance between the gate and the metal.

On claim 10: the method by Gaston et al further comprises scaling the test structure capacitance based on at least one scaling dimension (size) associated with the design structure (see Table 1 and "Determination of optimum structure").

On claim 12: because the RAPHAEL simulation tool as applied to optimize the test structure by Gaston et al (cf. page 159 and reference 2 on page 160) is a finite difference method applied to a differential formulation it inherently needs geometric boundary conditions because said geometric boundary conditions are the integration constants of the solution of the differential equations. Therefore, the method by Gaston et al meets claim 12.

On claim 26: Gaston et al teach a method of determining a capacitance for use in a circuit simulation, the method comprising: selecting a design structure at least partially defined by one or more design structure parameters (final paragraph of page 159; said "one or more design structures" comprising track spacing (cf. loc.cit., lines 12-14)); determining a design structure capacitance of the design structure (through RAPHAEL; see Figure 5 and loc.cit.); determining a desired test structure capacitance based on the one or more design structure parameters (the design structure selection is aimed at optimization of the test structure (see final paragraph of page 159, first five lines) and the test structure data (in particular the FIB measurement results of the thickness of the dielectric (page 158, first column, final paragraph, and page 159, final paragraph, lines 6-12)) including information regarding a plurality of test structures (differing at least in their track spacing; see page 159, final paragraph, lines 11-13), the information including a test structure capacitance (the capacitance plotted in Figure 5 as a function inter alia of said track spacing) and one or more test structure parameters associated with each of the plurality of test structures (namely at least said track spacing test structure parameter; see Figure 5); and calculating a parasitic capacitance of the design structure, wherein calculating the parasitic capacitance comprises deducting the desired test structure capacitance from the design structure capacitance: because the parasitic capacitance aimed at here is the capacitance other than the true M_2/M_1 capacitance obtained through FIB measurements (final paragraph of first column of page 158) and the parasitic capacitance is that part of the capacitance that is the contribution from neighboring conductive portions of the device interacting over distance the parasitic

capacitance is obtained by deducting the test structure capacitance from the design structure capacitance. In conclusion, Gaston et al anticipate claim 26.

On claim 29: the test structure capacitance associated with each of the plurality of test structures is determined by simulating each test structure (page 159, second column, final paragraph, lines 6-9); extracting a test structure capacitance of each simulated test structure (through the application of parasitic capacitance extraction program RAPHAEL; loc.cit.); and scaling each test structure based on at least one scaling dimension associated with the design structure (namely size: see Table 1 and "Determination of optimum structure").

On claim 31: the test structure in the method by Gaston et al further includes an empirical device capacitance associated with each of the plurality of test structures determined by physically testing each of the test structures (the large parallel plate capacitance as determined by FIB measurements of the thickness of the dielectric layer: see page 158, first column, final paragraph), wherein the method further includes: determining a desired empirical device capacitance based on the one or more design structure parameters and the test structure data (test structure data on capacitance as function of size, see Table 1); and calculating a total capacitance of the design structure (through RAPHAEL: see page 159, final paragraph), wherein calculating the total capacitance inherently comprises adding the parasitic capacitance to the desired empirical device capacitance because parasitic capacitance is by definition that part of the capacitance of the device that is an unwanted consequence of the neighboring conductive portions of the device interacting over distance.

On claim 32: the method by Gaston et al, in particular the determination of the test structure capacitance associated with each of the plurality of test structures is determined by physically testing the test structure (through FIB as applied to the dielectric layer; see page 158, first column, final paragraph).

On claim 33: in the method by Gaston et al the design structure capacitance is determined by simulating the design structure (through the use of simulation package RAPHAEL: see page 159, final paragraph); and extracting a design structure capacitance of the simulated design structure (RAPHAEL is a parasitic capacitance extraction tool).

On claim 35: in the method by Gaston et al at least one of the one or more design structure parameters is different from at least one of the one or more test structure parameters associated with each of the plurality of test structures because a test structure capacitance is a capacitance of an actual device while a design structure capacitance is a capacitance of a virtual device (that they may have different or identical values is another matter), and wherein determining the desired test structure capacitance comprises using an algorithm to determine a desired test structure capacitance, namely the TCAD simulation tools used in the optimization of the test structure capacitance (see page 159, final paragraph).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 3, 7, 30 and 34*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaston et al (Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Volume 8, March 1995) in view of Kim et al (IEEE Transactions on Components and Packaging Technologies, Volume 23, No. 1, March 2000). *As detailed above*, Gaston et al anticipate claims 1, 2, 29 and 33. *Gaston et al do not specifically* teach the step of extracting the test structure capacitance (claim 3 and claim 30) or the design structure capacitance (claim 7 and claim 33) to comprise using three-dimensional capacitance field solving. However, it would have been obvious to include either of these two steps as claimed in view of Kim et al, who, in a simulation to obtain a capacitance in a CMOS integrated circuit (cf. abstract) teach to employ a three-dimensional version of RAPHAEL (cf. page 185, first column, second paragraph), a parasitic capacitance simulation package (see references 14 and 15 on page 188), for said simulation for the specific purpose of achieving a full simulation (cf. abstract) thus extracting the test structure capacitance (thus meeting claim 3) from a computer-simulated extraction of said design structure capacitance (thus meeting claim 7). *Motivation* for inclusion of the teaching by Kim et al within the context of Gaston et al derives from the obvious increase in the reliability of three-dimensional simulation over simulation in any lower dimension, considering the inherently three-dimensional nature of any integrated circuit. *Combination* of the teachings merely requires at most replacing version 2.2 as referred to by Gaston et al (see their reference 2) by the referred-to

three-dimensional version (cf. reference 15 in Kim et al). *Success* of the implementation of said combination can therefore be reasonably expected.

5. ***Claims 11 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaston et al (Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Volume 8, March 1995) in view of Anholt et al (IEEE Transactions on Microwave Theory and Techniques, Volume 39, No. 7, July 1991). As detailed above, Gaston et al anticipate claim 10. *Although the design structure (ULSI CMOS process integrated circuit) of the method by Gaston et al does comprise a gate (see third paragraph of second column of page 157) Gaston et al do not necessarily teach* the further limitation that the at least one scaling dimension to comprise the width of the gate. *However, it would have been obvious* to include said further limitation in view of Anholt et al, who, in a patent on parasitic capacitance extraction in field effect transistors, hence analogous art, teach the width of the field effect transistor as a scaling dimension associated with the design structure (fourth paragraph of second column of page 1247), which logically implies the gate width to be a scaling dimension associated with the design structure as well, because scaling in a certain coordinate implies the scaling of each and every length along said coordinate including the gate width of said field effect transistor (see line 7 of second column of 1247). *Motivation* to include the further limitation as taught by Anholt et al in the invention by Gaston et al derives from the increasing importance of parasitic capacitance with decreasing gate width, as explained by Anholt et al (first paragraph of first column of page 1247).

On claim 15: the rejection under 35 USC 103(a) made here is provided subject to the best understanding by the examiner given the indefiniteness noted under 35 USC 112, second paragraph as expressed above. As detailed above, Gaston et al anticipate claim 12. Gaston et al do not necessarily teach the further limitation as defined by claim 15, although Gaston et al do teach to take into account capacitances of conductive layers in both vertical and horizontal directions (see Figure 1 and page 157, first column, "Introduction"). However, it would have been obvious to include said further limitation in view of Anholt et al, who, in a patent on parasitic capacitance extraction in field effect transistors, hence analogous art, teach the application of both measurement and analysis to a field effect transistor taking explicitly into account capacitances due to source-drain separations (see page 1249, first column, central paragraph). Motivation to include the teaching by Anholt et al in this regard in the invention by Gaston et al stems from the presence of "fine pitch" metallization layers (see Gaston et al, page 157, first column), i.e., short-channel, field effect transistors in many ULSI integrated circuits while the capacitances associated with gate and source and drain regions as analyzed and measured by Anholt et al form obvious topics of applications for the method by Gaston et al, directed as the latter is to parasitic capacitances of metal traces (see Figure 1).

6. ***Claims 13-14, 21, 23- 24, 27-28*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaston et al (Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Volume 8, March 1995) in view of Long et al (6,169,302 B1). As

detailed above, Gaston et al anticipate claim 12. *Although the design structure (ULSI CMOS process integrated circuit) of the method by Gaston et al does comprise a gate (see third paragraph of second column of page 157) Gaston et al do not necessarily teach* the further limitation as defined by claim 13. However, it would have been obvious to include said further limitation in view of Long et al, who, in a patent drawn to a method to determine the parasitic capacitance between the gate and the drain-source local interconnect in a field effect transistor (hence closely related art) teach the parasitic capacitance to be predominantly determined by the gate to source, - hence gate to source-drain active area, overlap (cf. col. 1, line 67 – column 2, line 5) in the specifically referred-to case of scaled-down device dimensions. *Motivation* for the inclusion of the teaching by Long et al in the method by Gaston et al thus derives from the increasing importance if not predominance of the contribution of said overlap between gate and source-drain active area to the overall parasitic capacitance, which Gaston et al aim to determine by their method.

On claim 14: the CMO(xide)S process integrated circuit by Gaston et al inherently has a gate oxide layer, and although the geometric boundary conditions inherent in the RAPHAEL method (see discussion of claim 12) necessarily must include the thickness of the dielectric for a given structure with capacitance (see page 158), *Gaston et al do not necessarily teach* said structure to be the capacitor formed by the gate to source overlap, in which case the thickness of the dielectric would be the thickness of the gate oxide, *although* when this would be so the thickness of the gate

oxide would necessarily be included in the boundary conditions inherent in the finite difference method by Raphael (see discussion of claim12).

However, it would have been obvious to include said further limitation in view of Long et al, who, in a patent drawn to a method to determine the parasitic capacitance between the gate and the drain-source local interconnect in a field effect transistor (hence closely related art) teach the parasitic capacitance to be predominantly determined by the gate to source, - hence gate to source-drain active area, overlap (cf. col. 1, line 67 – column 2, line 5) in the specifically referred-to case of scaled-down device dimensions. *Motivation* for the inclusion of the teaching by Long et al in the method by Gaston et al thus derives from the increasing importance if not predominance of the contribution of said overlap between gate and source-drain active area to the overall parasitic capacitance, which Gaston et al aim to determine by their method.

On claim 21: Gaston et al teach a method of determining a capacitance for use in a circuit simulation, the method comprising: selecting a test structure (the true M_2/M_1 capacitance in a ULSI integrated circuit; see pages 157-158, particularly second column of page 157 and first paragraph as well as final paragraph of the first column of page 158) inherently based on one or more geometric boundary conditions (the boundary conditions for the electromagnetic field at the interface between conducting and insulating components of the test structure capacitance) associated with a design structure (see page 159, final paragraph); simulating the test structure (see page 159, final paragraph); extracting a test structure capacitance of the simulated test structure

(see the third and fourth sentence of second column of page 159); extracting a test structure capacitance of the simulated test structure (namely: the parasitic capacitance of said test structure (final paragraph of second column of page 159)); simulating the design structure (using simulation program RAPHAEL which is by definition and capabilities a simulation package for the simulation of (parasitic) capacitance in a design structure; see final paragraph of page 159); extracting a design structure capacitance of the simulated design structure (RAPHAEL is an parasitic capacitance extraction simulation tool; loc.cit.); scaling the test structure capacitance based on at one scaling dimension associated with the design structure (see Table 1 and "Determination of optimum structure"); and calculating a parasitic capacitance of the design structure, wherein calculating the parasitic capacitance comprises deducting the test structure capacitance from the design structure capacitance (because the parasitic capacitance aimed at here is the capacitance other than the true M_2/M_1 capacitance obtained through FIB measurements (final paragraph of first column of page 158) and the parasitic capacitance is that part of the capacitance that is the contribution from neighboring conductive portions of the device interacting over distance the parasitic capacitance is obtained by deducting the test structure capacitance from the design structure capacitance).

Although the design structure (ULSI CMOS process integrated circuit) of the method by Gaston et al does comprise a gate (see third paragraph of second column of page 157) Gaston et al do not necessarily teach the further limitation that the test structure comprises also a source-drain active area, a contact and a metal, and that the

test structure capacitance comprises a gate to source-drain capacitance between the gate and the source-drain active area, a gate to contact capacitance between the gate and the metal, and a gate to metal capacitance between the gate and the metal. *However, it would have been obvious to include* said further limitation in view of Long et al, who, in a patent drawn to a method to determine the parasitic capacitance between the gate and the drain-source local interconnect in a metal-on-semiconductor field effect transistor (i.e., MOSFET) (hence closely related art). Said MOSFET inherently comprises a source-drain active area, a metal and contact to either source or drain electrodes. Said MOSFET also inherently as test structure capacitance comprises a gate to source-drain capacitance (capacitances 120 and 122 in Figure 1) between the gate and the source-drain active area, a gate to contact capacitance between the gate and the tungsten contacts (see gate-to-contact-capacitances 130 and 132 in Long et al. and column 1, line 58 – column 2, 5; and column 4, 8-38). *Motivation* to include said teaching by Long et al is found in the application of the relatively more generically described method by Gaston et al to the frequently occurring case of MOSFETs, thus enlarging the area of application of the invention, while the gate-to-contact capacitances are of increasing importance in scaled-down devices (see statement by Long et al, column 1, line 58 – column 2, line 5) including ULSI integrated circuits (as taught by Gaston et al).

On claim 23: Although Gaston et al do not necessarily teach the further limitation as defined by claim 23 it would have been obvious to include said further limitation in view of Long et al, who, in a patent drawn to a method to determine the parasitic

capacitance between the gate and the drain-source local interconnect in a field effect transistor (hence closely related art) teach the parasitic capacitance to be predominantly determined by the gate to source, - hence gate to source-drain active area, overlap (cf. col. 1, line 67 – column 2, line 5) in the specifically referred-to case of scaled-down device dimensions. *Motivation* for the inclusion of the teaching by Long et al in the method by Gaston et al thus derives from the increasing importance if not predominance of the contribution of said overlap between gate and source-drain active area to the overall parasitic capacitance, which Gaston et al aim to determine by their method.

On claim 24: the CMO(xide)S process integrated circuit by Gaston et al inherently has a gate oxide layer, and although the geometric boundary conditions inherent in the RAPHAEL method (see discussion of claim 12) necessarily must include the thickness of the dielectric for a given structure with capacitance (see page 158), *Gaston et al do not necessarily teach* said structure to be the capacitor formed by the gate to source overlap, in which case the thickness of the dielectric would be the thickness of the gate oxide, *although* when this would be so the thickness of the gate oxide would necessarily be included in the boundary conditions inherent in the finite difference method by Raphael.

However, it would have been obvious to include said further limitation in view of Long et al, who, in a patent drawn to a method to determine the parasitic capacitance between the gate and the drain-source local interconnect in a field effect transistor (hence closely related art) teach the parasitic capacitance to be predominantly

determined by the gate to source, - hence gate to source-drain active area, overlap (cf. col. 1, line 67 – column 2, line 5) in the specifically referred-to case of scaled-down device dimensions. *Motivation* for the inclusion of the teaching by Long et al in the method by Gaston et al thus derives from the increasing importance if not predominance of the contribution of said overlap between gate and source-drain active area to the overall parasitic capacitance, which Gaston et al aim to determine by their method.

On claim 27: Gaston et al do not necessarily teach the further limitation as defined by claim 27. *However, it would have been obvious* to include said further limitation in view of Long et al, who teach

(a) the design structure to comprise a design structure gate 210 and a design structure contact (either 206 or 208), and the one or more design structure contacts comprise(s) a distance between the design structure gate and the design structure contact (230 or 232) (cf. column 4, lines 40-55, and column 6, lines 15-22). *Motivation* to include said further limitation as taught by Long et al in the invention by Gaston et al is the increasing importance of gate-to-contact capacitance with reduction of the physical proportions of the device (cf. column 1, line 58 – column 2, line 5 in Long et al, while Gaston et al indeed aims at ULSI integrated circuits ULSI means ultra-large-scale-integration hence small physical dimensions (cf. page 157, second column, third paragraph);

(b) each of the plurality of test structures to comprise a test structure gate 112 and a test structure contact (114 or 116) (cf. column 1, lines 15-30 and column 4, lines

8-11), and the one or more test structure parameters associated with each of the plurality of test structures comprises a distance between the test structure gate and the test structure contact, namely the distance between said gate 112 and either interconnects 114 or 116 (cf. Figure 1). In this regard Long et al is merely more explicit in what can be expected in a CMOS process integrated circuit because any MOS transistor meets the further limitation ad (b). Motivation, to include the teaching by Long et al in this regard in the invention by Gaston et al, stems from the straightforward applicability to the large class of actual (C)MOS transistors of the invention by Gaston et al.

On claim 28: although Gaston et al do not necessarily teach the further limitation of claim 28 they do include in their design structure the distance between trace 1 and trace 3 (corresponding to the distance between source and drain interconnects 206 and 208 in the specific application by Long et al: see Figure 2 in Long et al and Figure 1 in Gaston et al), while each of the plurality of test structures comprises a test structure first contact 114 and a test structure second contact 116 (Figure 1 in Long et al; column 1, lines 15-30 and column 2, lines 5-10). Specific application of the teaching by Gaston et al to the example of MOS field effect transistor as rendered obvious by Long et al as discussed above thus immediately meets the claim. *Motivation*, to include the teaching by Long et al in this regard in the invention by Gaston et al, stems from the straightforward applicability to the large class of actual (C)MOS transistors of the invention by Gaston et al (page 157, second column) for which a more accurate

extraction of parasitic capacitance is of increasing importance for reduced physical dimensions (see column 1, line 58 – column 2, line 5 in Long et al).

7. ***Claims 16 and 18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaston et al (Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Volume 8, March 1995) in view of You et al (6,449,754 B1). As detailed above, Gaston et al anticipate claim 1. With reference to the noted indefiniteness in the sense of 35 USC 112, second paragraph, the following rejection is offered. *Gaston et al do not necessarily teach* the further limitation defined by claim 16. *However, it would have been obvious to include said further limitation* in view of *You et al*, who, in a patent drawn to a method of measuring the accuracy of parasitic capacitance extraction (cf. title), - hence closely related art, teach providing a calibration structure (namely: the capacitive element having the highest weight factor"; cf. abstract) inherently having one of more boundaries; determining a target calibration structure capacitance of the calibration structure (namely: the capacitance of said calibration structure; cf. abstract: "extracted values of the individual capacitance elements"..."with the error in each element being influence by a weight factor"); simulating the calibration structure (cf., column 1, lines 38-59); extracting a test calibration structure capacitance of the simulated calibration structure using a first simulator (this is what the simulation does; loc. cit.; said first simulator being, e.g., a 3D field solver (column 1, lines 38-59); inherently the use of any calibration involves calculating the difference between a test item and the calibration item and determining if the difference is satisfactory according

to an accuracy criterion (cf. Stan Gibilisco, "The Illustrated Dictionary of Electronics", TAB Books, Division of McGraw-Hill, sixth edition, page 90: calibration: "Determining the degree to which the response of a circuit or device corresponds to desired performance"; "calibration accuracy: "the amount of agreement between the value of a quantity, as indicated by an instrument, and the true value, expressed as a percentage of error") (see also column 3, lines 39-53); upon which at least one of the one or more boundary conditions which match the boundary conditions pertinent to the test structure capacitance, including any adjusted boundary conditions, are to be changed following Gaston et al (page 159, second column, final paragraph; note that changing the track spacing implies a change in at least one of the boundary conditions, because of the change of the independent variable in said one of the boundary conditions, namely: the coordinate at the boundary) as an example of the reason for access for the purpose of circuit design indicated by You et al (column 7, lines 48-50). *Motivation* to include the teaching by You et al in this regard in the method by Gaston et al derives from the enhanced accuracy with which parasitic capacitance can be extracted (You et al, column 1, lines 5-7).

On claim 18: the target calibration structure in the method by Gaston et al and You et al is determined by physically testing the calibration structure (the capacitive element used for calibration is a member of the set of individual capacitance elements subjected to the measuring technique taught by You et al (cf. abstract)). *Motivation* to include the teaching by You et al follows from the resulting increase in accuracy with which the parasitic capacitance can be extracted (You et al, column 1, lines 5-7):

calibration structures require extraordinary accuracy exactly because they are used for calibration.

8. ***Claims 22 and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaston et al and Long et al as applied to claim 21 above, and further in view of Anholt et al (IEE Transactions on Microwave Theory and Techniques, Volume 39, No. 7, July 1991, pp. 1247-1251). As detailed above, claim 21 is unpatentable over Gaston et al in view of Long et al. Neither necessarily teach the further limitation as defined by claim 22. *However, it would have been obvious* to include said further limitation in view of Anholt et al, who, in a patent on parasitic capacitance extraction in field effect transistors, hence analogous art, teach the width of the field effect transistor as a scaling dimension associated with the design structure (fourth paragraph of second column of page 1247), which logically implies the gate width to be a scaling dimension associated with the design structure as well, because scaling in a certain coordinate implies the scaling of each and every length along said coordinate including the gate width of said field effect transistor (see line 7 of second column of 1247). *Motivation* to include the further limitation as taught by Anholt et al in the invention by Gaston et al derives from the increasing importance of parasitic capacitance with decreasing gate width, as explained by Anholt et al (first paragraph of first column of page 1247).

On claim 25: the rejection under 35 USC 103(a) made here is provided subject to the best understanding by the examiner given the indefiniteness noted under 35 USC 112, second paragraph as expressed above. As detailed above, Gaston et al anticipate claim 12. Gaston et al do not necessarily teach the further limitation as defined by claim

15, although Gaston et al do teach to take into account capacitances of conductive layers in both vertical and horizontal directions (see Figure 1 and page 157, first column, "Introduction"). However, it would have been obvious to include said further limitation in view of Anholt et al, who, in a patent on parasitic capacitance extraction in field effect transistors, hence analogous art, teach the application of both measurement and analysis to a field effect transistor taking explicitly into account capacitances due to source-drain separations (see page 1249, first column, central paragraph). Motivation to include the teaching by Anholt et al in this regard in the invention by Gaston et al stems from the presence of "fine pitch" metallization layers (see Gaston et al, page 157, first column), i.e., short-channel, field effect transistors in many ULSI integrated circuits while the capacitances associated with gate and source and drain regions as analyzed and measured by Anholt et al form obvious topics of applications for the method by Gaston et al, directed as the latter is to parasitic capacitances of metal traces (see Figure 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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